Marvell Delivers Industry's First Dual 400GbE PHY With 100G Serial I/Os And MACsec Security For High-Density Implementations In The Data Center And Cloud

Further Advances Marvell's Leadership in PHY Connectivity Solutions with High-Speed SerDes Technology

SANTA CLARA, Calif., March 9, 2020 /PRNewswire/ -- Marvell (NASDAQ: MRVL) today introduced the industry's first dual 400GbE (Gigabit Ethernet) PHY transceiver with 100GbE serial electrical I/O capabilities, designed to drive next-generation, secured high-density optical infrastructure. Data growth continues to put unprecedented demand on data centers and cloud providers, spurring the need for innovative technologies that can provide higher throughputs with enhanced energy efficiency. Marvell's new PHY device with 100G serial I/Os enables the doubling of faceplate bandwidth on datacenter networks while reducing the total power consumption and cost per bit. The new device offers 256-bit MACsec encryption to ensure heightened point-to-point security, Class C compliant precision time protocol (PTP) timestamping for enhanced synchronization and Marvell's industry-leading 112G PAM4 SerDes technology for high-density 400GbE and 100GbE deployments.

The advent of 100G serial electrical signaling optical modules will allow 1:1 mapping between electrical and optical I/O speeds. This removes the additional circuitry inside 400GbE optical modules to convert from 50G electrical I/Os to 100G per lambda optical I/Os, reducing cost and power. As first to market with a PHY transceiver that has 100G serial I/Os, Marvell is placing itself at the forefront of this transitional process. The new PHY transceivers provide networking OEMs with the cutting-edge technology required for high-density dual 400G/octal 100G optical modules in QSFP-DD and OSFP form factors for cloud and data center applications.

Marvell's newest dual 400GbE MACsec PHY, the 88X9121P, enables interfacing between the current generation of switch ASICs with the next generation of optics and vice versa by supporting translation between 50G PAM4 and 100G PAM4 based implementations of 400GbE, 200GbE and 100GbE. The 88X9121P is both footprint- and software-compatible with the recently announced 88X7121P, providing a seamless upgrade path that facilitates migration to modules with 100GbE serial I/Os.

"We see the introduction of our feature-rich 100G serial I/O based, dual 400GbE PHYs playing a major role in the next evolutionary phase of the global data center and cloud sectors," said Faraj Aalaei, executive vice president of the Networking Business Group at Marvell. "The transition to 100G serial signaling is critical for high-density optical interconnects required for next-generation switching solutions. Our newest PHY transceivers will help drive the industry transition to 100G serial I/O-based optics as data centers and cloud providers look to bring greater computing bandwidth and efficiency to their customers."

"Marvell has a rich history of innovation in SerDes technology that is further strengthened by our SoC design and Ethernet expertise," said Sandeep Bharathi, senior vice president of Central Engineering at Marvell. "Our newest PHY transceiver device extends Marvell's SerDes technology leadership by integrating our state-of-the-art 112G PAM4 SerDes solution in advanced FinFET process into the industry's first dual 400GbE MACsec PHY with 100GbE serial I/Os."

"We see 100Gbps serial I/O as a foundational speed and expect it will enable 400GbE port shipments to reach 6.5 million by 2023," said Bob Wheeler, principal analyst for networking at The Linley Group. "Marvell's new PHY is a milestone in kickstarting the ramp of 100Gbps-serial-electrical optics and will help accelerate the deployment of 400GbE in cloud data centers."

The 88X9121P is the latest addition to Marvell's popular Alaska ® C Ethernet transceiver family. It is fully compliant with IEEE standards for 400GbE, 100GbE and 50GbE, and exceeds the electrical specifications to interface with QSFP-DD and OSFP optical modules. The 88X9121P's IEEE 802.1AE 256-bit MACsec encryption for point-to-point links provides enhanced security and allows for flexible deployment of MACsec encryption without incurring the cost and power burden of including this functionality in the switch ASIC. The high-accuracy Class C PTP timestamping offered by this device delivers the elevated timing precision levels now being mandated by carriers and their network infrastructure partners.

The Marvell 88X9121P is currently sampling.

For more information on Marvell's 88X9121P PHY transceiver, please visit https://www.marvell.com/products/transceivers/alaska-c-gbe/88x9121p.html.

About Marvell
Marvell first revolutionized the digital storage industry by moving information at speeds never thought possible.

Today, that same breakthrough innovation remains at the heart of the company's storage, processing, networking, security and connectivity solutions. With leading intellectual property and deep system-level knowledge, Marvell's semiconductor solutions continue to transform the enterprise, cloud, automotive, industrial, and consumer markets. To learn more, visit: https://www.marvell.com/

Marvell Communications
Phone: +1 408 222 8966
Email: pr@marvell.com

View original content to download multimedia:http://www.prnewswire.com/news-releases/marvell-delivers-industrys-first-dual-400gbe-phy-with-100g-serial-ios-and-macsec-security-for-high-density-implementations-in-the-data-center-and-cloud-301019512.html

SOURCE Marvell

Additional assets available online: Photos (1)

https://investor.marvell.com/2020-03-09-Marvell-Delivers-Industrys-First-Dual-400GbE-PHY-with-100G-Serial-I-Os-and-MACsec-Security-for-High-Density-Implementations-in-the-Data-Center-and-Cloud