Marvell Enabling The Next Generation Of Data Center And Automotive AI Accelerator ASICs

Powering the industry's first peta OP/s AI accelerator-on-a-chip

SANTA CLARA, Calif., Sept. 29, 2020 /PRNewswire/ -- Marvell (NASDAQ: MRVL) today announced that the company's custom application-specific integrated circuits (ASICs) offering is well-positioned to enable the next generation of artificial intelligence (AI) accelerator solutions for the data center and automotive markets.

Marvell's custom ASIC offering is differentiated for AI and machine learning applications with leading density and performance SRAMs, the highest performance SerDes and a full spectrum of pre-qualified high-bandwidth memory interfaces. It also boasts the latest PCIe and IO technologies including custom multi-tap, multi-stage, and high-drive clock elements. This IP is designed and pre-qualified by Marvell to enable unparalleled performance and reliability.

Marvell's ASICs ensure fastest time to market with turnkey design and verification, as well as custom mesh interconnect network on chip communication. Additionally, Marvell's ASIC methodology features adaptive voltage supplies for power reduction along with custom hierarchical test methodology, logic redundancy and a custom memory BIST solution for enhanced reliability. Marvell supports various ASIC engagement models, from a full turnkey offering to a customer-owned physical design with the option for customers to optimize their own differentiating blocks. Regardless of the engagement model, Marvell provides a qualified flow from physical design, design for test, power and timing optimization, simulation, ATPG and manufacturing test, prototype bring-up, to ownership of reliability from the beginning to the end of life cycle.

Marvell is engaged with a number of data center and automotive manufacturers to develop custom AI ASICs. Groq, which expands Marvell's customer roster of innovative companies using its ASIC offerings, is creating the industry's first peta operations per second (POP/s) AI accelerator-on-a-chip.

"Our ASIC partnership with Marvell has led to truly extraordinary results," said Jonathan Ross, CEO of Groq. "We knew that to break free from the traditional architectures such as FPGAs, CPUs, and GPUs, and to build something revolutionary that the industry hadn't seen before was going to require a unique partner. Marvell helped us take our vision of the first and only peta operations per second capable processor and make it a reality. They're one of the select few ASIC teams that can both innovate, as well as deliver."

"These latest custom ASIC designs are the product of more than 25 years of ASIC design experience and leadership, enabling the most complex accelerator, storage and automotive solutions," said Kevin O'Buckley, general manager of the ASIC BU at Marvell. "Our unique IP, design, placement and test flow allow us to partner with our customers to create the industry's most complex and highest performance AI accelerator chips, delivered to market quickly."

Key elements of Marvell's design partnerships include hierarchical design implementation with abstraction and distributed compute, ultra-robust power distribution and power supply integrity modeling, custom hierarchical test methodology with logic redundancy, chip-wide useful-skew structured clock network for system and test clocks, a design profiling dashboard, and final netlist to tape out in under 85 days.

More information on Marvell's unique custom ASIC offering can be found here.

About Marvell
To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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