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Marvell Joins Universal Chiplet Interconnect Express Consortium

Brings Established Expertise in Multi-Chiplet, Cloud-Optimized Silicon Design to Open Industry Standards Collaboration

SANTA CLARA, Calif., June 8, 2022 /PRNewswire/ -- Marvell (NASDAQ: MRVL) today announced that the company has joined the Universal Chiplet Interconnect Express (UCIe) Consortium as part of its ongoing development of open chiplet interconnect standards. Marvell's contributions to the UCIe standard will leverage the company's advanced chiplet interconnect and packaging experience to help further the consortium's objective of developing open standards that create a more robust ecosystem for inter-operable chiplets.

Marvell's UCIe participation is complementary to the company's existing work in the Open Compute Project (OCP) and Optical Internetworking Forum (OIF) which is aimed at the development of open standards-based solutions for connecting single or multi-node 5nm and 3nm chiplets. Through these experiences, Marvell brings advanced domain knowledge and a unique perspective that will help align and optimize global chiplet interconnect standards for a range of leading-edge applications with differing requirements such as CXL, Ethernet and custom low-latency connectivity while fostering chiplet interoperability.

"Marvell has been an industry pioneer in chiplet connectivity and continues to push the envelope of performance optimization for a wide range of multi-chiplet applications in advanced packaging architectures," said Noam Mizrahi, Chief Technology Officer and Senior Fellow at Marvell. "We see the great value in aligning interconnect standards across the industry and look forward to contributing towards that goal as a member of the UCIe consortium."

"UCIe represents the culmination of years of learning and implementation experience with on-package interconnects at a time that is right for industry standardization," said Dr. Debendra Das Sharma, Intel Senior Fellow. "We are excited that Marvell has joined the consortium and is working to develop cloud-optimized multi-die solutions that are compatible with UCIe."

"The increasing complexity of data center SoCs elevates the importance of high-speed interconnect for massively complex multi-die designs with advanced packaging, where Marvell brings extensive expertise to UCIe," said Linley Gwennap, Principal Analyst, TechInsights. "Diverging and demanding requirements of emerging applications, including CXL and a range of low-latency use cases, underscores the importance of having both interoperable and application-optimized open chiplet interconnect standards."

For more information on Marvell's ASIC and SoC design capabilities, visit us at https://www.marvell.com/products/custom-asic.html

About Marvell

To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies over 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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